PATENT
Attorney Reference Number 1011-67625-01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Rajski et al.
Application No. 10/777,443
Filed: February 10, 2004
Confirmation No. Unknown
For: ARITHMETIC BUILT-IN SELF TEST OF MULTIPLE SCAN-BASED INTEGRATED CIRCUITS
Examiner: Unknown
Art Unit: Unknown
Attorney Reference No. 1011-67625-01

CERTIFICATE OF MAILING

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Attorney for Applicant(s) _____

Date Mailed May 7, 2004

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TRANSMITTAL LETTER

Enclosed for filing in the application referenced above are the following:

- ☒ Information Disclosure Statement
  - ☒ Form 1449
- ☒ Terminal Disclaimer
- ☒ A check in the amount of $110.00 to cover the Terminal Disclaimer fee.

☒ The Director is hereby authorized to charge any additional fees that may be required, or credit over-payment, to Deposit Account No. 02-4550. A copy of this sheet is enclosed.

☒ Please return the enclosed postcard to confirm that the items listed above have been received.

Respectfully submitted,

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INFORMATION DISCLOSURE STATEMENT FOR CONTINUING APPLICATIONS

Listed on the accompanying form PTO-1449 are several English-language documents. Applicants respectfully request that such documents be listed as references cited on the issued patent.

The present application relies upon U.S. Patent Application No. 09/276,474, which was filed March 25, 1999, for an earlier filing date under 35 U.S.C. § 120. Furthermore, documents listed on the accompanying form PTO-1449 were disclosed to or cited by the Patent Office in the earlier U.S. application.

If the present application was filed after June 30, 2003, copies of United States patents and United States published patent applications do not have to be provided to the Patent Office. This requirement of 37 C.F.R. § 1.98(a)(2)(i) has been waived by the United States Patent and Trademark Office pursuant to the Official Gazette Notice on August 5, 2003 (1276 OG 55).

Applicants will provide copies of such patents upon request.

Copies of the documents listed on the accompanying form PTO-1449 that were cited by applicants in the earlier application need not be sent to the Patent Office pursuant to 37 C.F.R. § 1.98. However, applicants will furnish the Patent Office with such copies upon request.

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The filing of this Information Disclosure Statement shall not be construed to be an admission that the information cited in the statement is, or is considered to be, prior art or otherwise material to patentability as defined in 37 C.F.R. §1.56.

Respectfully submitted,

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT		
	Attorney Docket Number	1011-67625-01
	Application Number	10/777,443
	Filing Date	February 10, 2004
	First Named Inventor	Rajski
	Art Unit	Unknown
	Examiner Name	Unknown

U.S. PATENT DOCUMENTS

NOTE: If this application was filed after June 30, 2003, copies of United States patents and United States published patent applications do not have to be provided to the Patent Office. This requirement of 37 C.F.R. § 1.98(a)(2)(i) has been waived by the United States Patent and Trademark Office pursuant to the Official Gazette Notice on August 5, 2003 (1276 OG 55).

Examiner's Initials*	Cite No. (optional)	Number	Publication Date	Name of Applicant or Patentee
		4,511,967	April 16, 1985	Witalka et al.
		4,947,395	August 7, 1990	Bullinger et al.
		5,226,149	July 6, 1993	Yoshida et al.
		5,239,262	August 24, 1993	Grutzner et al.
		5,369,646	November 29, 1994	Shikatani
		5,416,783	May 16, 1995	Broseghini et al.
		5,590,354	December 31, 1996	Klapproth et al.
		5,617,531	April 1, 1997	Crouch et al.
		5,724,603	March 3, 1998	Nishiguchi
		5,790,561	August 4, 1998	Borden et al.

Examiner's Initials*	Cite No. (optional)	OTHER DOCUMENTS
		Edirisooriya, et al., "Minimizing Testing Time in Scan Path Architecture," IEEE Circuits and Systems, 1992 Midwest Symposium, pages 1205-1207.
		Zacharia, et al., "Decompression of Test Data Using Variable-Length Seed LFSRs," Microelectronics and Computer Systems Laboratory, McGill University, Montreal, Canada.
		Adham, et al., "Arithmetic Built-in Self Test for Digital Signal Processing Architectures," in Proceedings of the IEEE 1995 Custom Integrated Circuits Conference, May 1-4, pages 29.6.0 - 29.6.4.

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		Application Number	10/777,443
		Filing Date	February 10, 2004
		First Named Inventor	Rajski
		Art Unit	Unknown
		Examiner Name	Unknown

		Rajski, et al., "On Linear Dependencies in Subspaces of LFSR-Generated Sequences," IEEE, Draft August 6, 1996, pages 0-11.
		Hurd, "Efficient Generation of Statistically Good Pseudonoise by Linearly Interconnected Shift Registers," IEEE Transactions on Computers, Vol. C-23, No. 2, February 1974, pages 146-152.
		Hellebrand, et al., "Pattern Generation for a Deterministic BIST Scheme," 1995 IEEE, pages 88-94.
		Rajski, et al., "Test Responses Compaction in Accumulators with Rotate Carry Adders," IEEE Transaction on CAD of Integrated Circuits and Systems, Vol. 12, No. 4, April 1993, pages 531-539.
		Rajski, et al., "Accumulator-Based Compaction of Test Responses," IEEE Transactions on Computers, Vol. 42, No. 6, June 1993, pages 643-650.
		Hellebrand, et al., "Built-in Test for Circuits with Scan Based on Reseeding of Multiple-Polynomial Linear Feedback Shift Registers," IEEE Transactions on Computers, Vol. 44, No. 2, February 1995, pages 223-233.

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